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10/766,161	01/28/2004	Robert Floyd Payne	TI-37352	3397

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EXAMINER	
GUARINO, RAHEL	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
11/05/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/766,161	PAYNE ET AL.	
	Examiner	Art Unit	
	Rahel Guarino	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/20/2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,3,5-8,14,18 and 20-23 is/are rejected.

7)☐ Claim(s) 11-13,15 and 17 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on 02/08/07. Claims 1, 3, 8, 11, 12, 14, 17, and 18 have been amended are pending on this application. Claims 2, 4, 9, 10, 16 and 19 have been cancelled.

Response to Arguments

2. Applicant should submit an argument under the heading "Remarks" pointing out disagreements with the examiner's contentions. Applicant must also discuss the references applied against the claims, explaining how the claims avoid the references or distinguish from them.

3. Applicant's arguments filed 8/20/2007 have been fully considered but they are not persuasive:

Applicant's arguments:

Claim 1, as amended, includes "... the analyzer component adjusts operation of the data clock and the transition clock according to the average operation of the set of consecutive bit times." Claim 18, as amended, includes "...adjusting data and transition clocks according to the determined average clock operation over the set of consecutive bit times." The references of record do not show, teach, or suggest the above recited limitations of claims 1 and 18. The Nakai reference fails to teach adjusting a data clock and a transition clock according to the average operation of the set of consecutive bit times.

Examiner's response:

Re claim 1 and 18, fig.1 shows the analyzer (element (10)) provides a moving average circuit (11a for clock component) and moving average circuit (11b for data component), where the input data is consecutive bits encoded by Manchester coding (col. 10 lines 24-56). The transition point extractor (12) receives input q6-0 from the moving average circuit and adjusts and corrects the shift difference of input waveform (col. 7 lines 21-50)

Applicant's arguments:

Claim 14, as amended, includes "... a data clock and a transition clock, wherein the sample component employs the data clock to obtain center samples and the transition clock to obtain edge samples; and wherein the analyzer component adjusts operation of the data clock and the transition clock according to the average operation of the set of consecutive bit times." The references of record do not show, teach, or suggest the above-recited limitations of claims 14.

Examiner's response:

Kim shows a data clock (fig.3 (dclk)) and a transition clock (fig.3 (eclk)), wherein the sample component (fig.3 (samplers(100)) employs the data clock to obtain center samples (col. 5 line 9-15) and the transition clock to obtain edge samples (col. 6 line 4-8), wherein an analyzer (fig.3 (90)) that generates an average operation for the set of consecutive bit (serial data "din" includes N-bits pattern, where each bit is contained within the bit time (same period)) (fig. 6; col. 7 lines 25-42). The CDR device recovers the sampling clock from the

incoming data transitions by placing the rising and falling of a clock signal in the middle of bit time.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1,3,5-7,18,20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. US, 7,076,377 in view of Nakai US, 6,370,212.

Re claim 1, Kim discloses a clock recovery device comprising (fig.3):

a sample component (100) that obtains center and edge samples of a serial data stream (din; col. 6 line 3-16).

a number of voting components (102) that identify early and late operation for a set of consecutive bit times of the serial data stream from the obtained center and edge samples (col. 6 line 16-22); a data clock (dclk) and a transition clock (eclk), wherein the sample component employs the data clock to obtain center samples (col. 5 line 9-15) and the transition clock to obtain edge samples (col. 6 line 4-8); does not teach an analyzer generates an average operation for the set of consecutive bit and wherein the analyzer component adjusts operation of the data clock and the transition clock according to the average operation of the set of consecutive bit times.

However, Nakai teaches an analyzer generates an average operation for

the set of consecutive bit (col. 9 line 14-30) and the analyzer adjusts operation of the data clock and the transition clock according to the average operation of the set of consecutive bit times (col. 4 line 20-26).

Therefore, taking the combined teaching of Kim and Nakai as a whole would have been rendered obvious to one skilled in the art to modify Kim to generate an average operation for the set of consecutive bit and adjusts operation of the data clock and the transition clock according to the average operation of the set of consecutive bit times for the benefit of extracting the clock component from the data (col. 12 line 66 to col. 13 line 7).

Re claim 3, the modified invention as claimed in claim 2, wherein the center samples are obtained on a rising edge of the data clock and the edge samples are obtained on a rising edge of the transition clock (col. 6 line 4-16,"Kim").

Re claim 5, the modified invention as claimed in claim 1, wherein the set of consecutive bit times comprises 8 bits (col. 6 line 53-56,"Nakai").

Re claim 6, the modified invention as claimed in claim 1, wherein the set of consecutive bit times comprises 16 bits (fig.7;"Nakai").

Re claim 7, the modified invention as claimed in claim 1 (fig.3), wherein the number of voting components respectively obtain a previous center sample, a current edge sample, and a current center sample from the sample component (121, 120; col. 6 line 5-16,"Kim") for one of the consecutive bit times and identify early and late operation for the one bit time according to the previous center

sample, the current edge sample, and the current center sample (col. 6 line 16-25,"Kim").

Re claim 18, Kim discloses a method of detecting early/late operation of clocks comprising (fig.3):

obtaining center and edge samples of a received serial data stream for a set of consecutive bit times according to data and transition clocks (col. 6 line 16-22);

analyzing the set of consecutive bit times to identify late operation(s) of the clocks within the respective consecutive bit times according to the obtained center and edge samples (col. 6 line 16-25);

analyzing the set of consecutive bit times to identify early operation(s) of the clocks within the respective consecutive bit times according to the obtained center and edge samples (col. 6 line 16-24); does not teach an average operation for the set of consecutive bit and adjusting data clock and the transition clock according to the average operation of the set of consecutive bit times.

However, Nakai teaches teach an average operation for the set of consecutive bit an average operation for the set of consecutive bit (col. 9 line 14-30) and adjusting data clock (col. 13 line 10 to col. 14 line 11) and the transition clock according to the average operation of the set of consecutive bit times (col. 9 line 41 to col. 10 line 30).

Therefore, taking the combined teaching of Kim and Nakai as a whole would have been rendered obvious to one skilled in the art to modify Kim to compare the identified late operation(s) with the identified early operation(s) and

adjusting data clock and the transition clock according to the average operation for the benefit of extracting the clock component from the data (col. 12 line 66 to col. 13 line 7).

Re claim 20, the modified invention as claimed in claim 18, wherein obtaining center samples comprises sampling the received serial data stream on rising edges of a data clock (col. 5 line 9-15 "Kim").

Re claim 21, the modified invention as claimed in claim 20 (fig. 3), wherein obtaining edge samples comprises sampling (sampling using data/edge samplers (100)) the received serial data stream (din) on rising edges of a transition clock (col. 6 line 3-16, "Kim").

Re claim 22, the modified invention as claimed in claim 18, wherein analyzing the set of consecutive bit times to identify late operation(s) comprises identifying a transition between a current edge sample and a previous center sample for each bit time (col. 6 line 16-25, "Kim");

Re claim 23, the modified invention as claimed claim 18, wherein analyzing the set of consecutive bit times to identify early operation(s) comprises identifying a transition between a current edge sample and a current center sample for each bit time (col. 6 line 16-24, "Kim").

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. US, 7,076,377 in view of Li et al. US, 6,693,985.

Re claim 8, Kim discloses a voting component comprising (fig.3), does not explicitly teach a sample input node.

However, Li teaches a current center sample input node (100) that receives a current center sample (col. 2 line 54-57); a current edge sample input node (101) that receives a current edge sample; a previous center sample input node (102) that receives a previous center sample; an early output node that selectively draws a reference current according to the current center sample, the current edge sample, and the previous center sample; a late output node that selectively draws the reference current according to the current center sample, the current edge sample, and the previous center sample (col. 5 line 1-30,"Li"); and circuitry for selectively controlling the early output node and the late output node (col. 5 line 34-39,"Li"); a complement center sample node that receives a logical complement of the current center sample; a complement edge sample node that receives a logical complement of the edge center sample; a complement previous sample node that receives a logical complement of the current previous sample; (col. 5 lines 19-36,"Li").

Therefore, taking the combined teaching of Kim and Li as a whole would have been rendered obvious to one skilled in the art to modify Kim to use a

sample input node and the control signal for the benefit of synchronizing the sampling signal (col. 3 line 40-48,"Li").

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. US, 7,076,377 in view of Garlepp et al. US, 6,920,622.**

Re claim 14, Kim discloses a clock recovery device comprising (fig.3):

a sample component (100) that obtains center and edge samples of a serial data stream (din; col. 6 line 3-16);

a number of voting components (100) that identify early and late operation for a set of consecutive bit times of the serial data stream from the obtained center and edge samples (col. 6 line 16-22);

a data clock (dclk) and a transition clock (eclk), wherein the sample component employs the data clock to obtain center samples (col. 5 line 9-15,"Kim") and the transition clock to obtain edge samples (col. 6 line 4-8,"Kim");does not teach an analyzer selectively draw a reference current at early and late output nodes.

However, Nakai teaches an analyzer selectively draw a reference current

at early and late output nodes according to the identified operation (fig.7; col. 7 line 44-59).

an analyzer (704,"Garlepp") that measures and compares current drawn by the number of voting components at the early and late output nodes and indicates an average operation based upon the comparison (col. 7 line 35-40, "Garlepp").

Therefore, taking the combined teaching of Kim and Garlepp as a whole would have been rendered obvious to one skilled in the art to modify Kim to measure and compare current for the benefit of increasing and decreasing by the appropriate offset (col. 7 line 63-65,"Garlepp").

Allowable Subject Matter

5. Claim 11-13, 15 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rahel Guarino whose telephone number is 571-270-1198. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Payne David can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RG

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SUPERVISORY PATENT EXAMINER